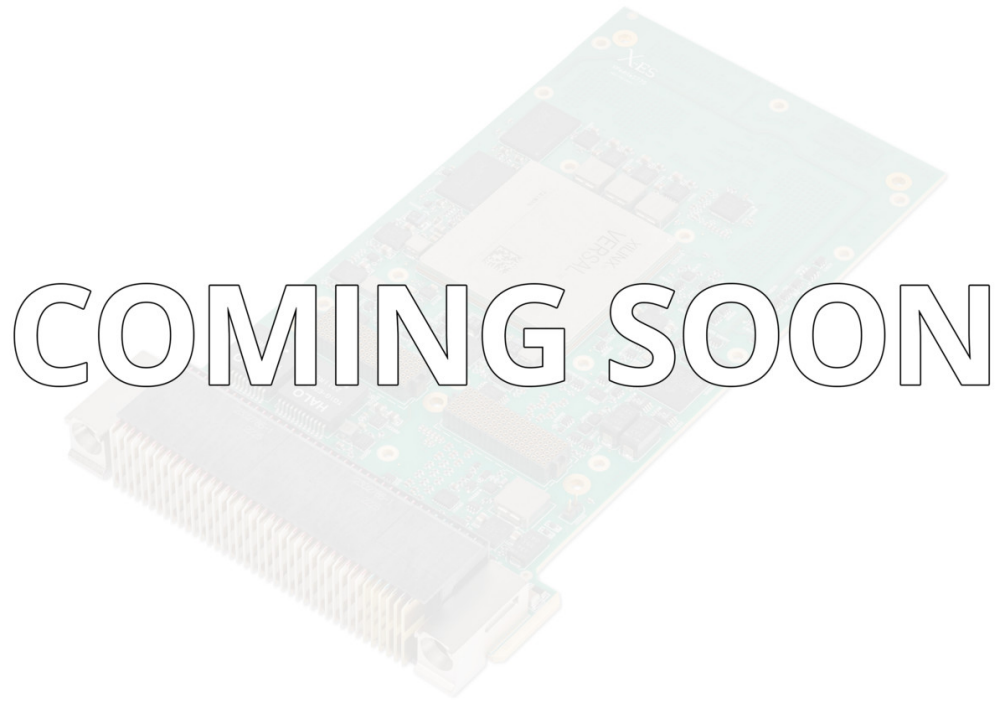
XPedite2870

AMD (formerly Xilinx) Versal® Gen 2 ASoC-Based 3U VPX Module with 32 GB of LPDDR5x, PCIe Gen5, and SecureCOTS™

- AMD (formerly Xilinx) Versal® Gen 2 AI Edge 2VE3858 or Prime 2VM3858 adaptive SoC
- Conduction-cooled 3U VPX (VITA 46) module
- Compatible with multiple VITA 65 OpenVPX™ slot profiles and SOSA-aligned options
- 32 GB of LPDDR5x SDRAM with in-band ECC
- 4 Gbit of OSPI FPGA configuration flash
- Up to 256 GB of UFS NAND flash
- XMC site with one x4 PCI Express Gen5-capable interface and rear I/O support
- Two x1 HSS 25 Gbps-capable interfaces to support 25GBASE-R Ethernet
- Two x4 HSS 25 Gbps-capable interfaces to support Ethernet, PCIe, etc.
- Interfaces on P1.A and P1.B can be combined to function as one x8 PCI Express interface
- One x1 HSS 8 Gbps-capable interface to support storage
- One DisplayPort 1.4 interface
- Two 10/100/1000BASE-T Ethernet ports
- One RS-232/422/485 serial port
- One UART/RS-232 maintenance port
- 14 LVDS GPIO (X5IO)
- 16 single-ended GPIO (HDIO) and three single-ended GPIO (MIO)
- Pinout compatible with SOSA I/O Intensive profile (SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16)
- SOSA-aligned to AMPS profile MODA3-16.2.15-1-F2C-(P4F)(P4F)(2E7-E3)(N-D1-U1-N-M3/M4/M5-N)
- FPGA Development Kit (FDK)
- Linux Yocto support
- Contact factory for information regarding support for 2VE3558, 2VM3558, and 2VM3654 ASoC SKUs



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The XPedite2870 is a high-performance, reconfigurable, conduction-cooled 3U VPX processing module based on the AMD Versal® Gen 2 adaptive system-on-chip (ASoC). With multiple high-speed fabric interfaces and 32 GB of four-channel LPDDR5x SDRAM with in-band ECC, the XPedite2870 is well suited for customizable, high-bandwidth signal-processing applications. It combines X-ES SecureCOTS™ technology with either a Versal Gen 2 AI Edge 2VE3858 or Prime 2VM3858 ASoC, enabling custom functions that help protect data from unauthorized modification or observation. This makes the XPedite2870 an ideal platform for applications with stringent security requirements.

The module provides a pinout compatible with the Sensor Open Systems Architecture (SOSA) I/O Intensive profile SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16) and is also designed to support SOSA-aligned AMPS profile MODA3-16.2.15-1-F2C-(P4F)(P4F)(2E7-E3)(N-D1-U1-N-M3/M4/M5-N).

As a heterogeneous compute platform, the XPedite2870 combines eight Arm Cortex®-A78AE application processor cores, 10 Arm Cortex-R52 real-time processor cores, a quad-core Arm Mali™-G78AE GPU, a high-bandwidth Network-on-Chip (NoC) interconnect, and a large programmable-logic fabric. When configured with the Versal Gen 2 AI Edge device, the platform also incorporates AI Engines that provide additional acceleration for machine-learning inference, signal processing, and other highly parallel compute workloads. These specialized processing resources support demanding applications including packet processing, signal processing, sensor I/O, DSP-intensive workloads, next-generation 5G wireless infrastructure, image classification, real-time situational awareness, and aerospace and defense systems.

For high-speed connectivity, the XPedite2870 provides two x4 and two x1 High-Speed Serial (HSS) interfaces capable of operating at up to 25 Gbps, along with two 10/100/1000BASE-T Ethernet ports. The module supports up to 256 GB of onboard NAND flash and provides a broad range of additional backplane I/O, including LVDS, single-ended GPIO, and RS-232/422/485 serial interfaces.

An integrated XMC site provides additional expansion capability. The XMC interface includes one x4 PCI Express Gen5-capable connection, capable of operating at up to 32 Gbps to the Versal Gen 2 ASoC, as well as X12d I/O routed directly to the VPX backplane connectors. Optional configurations can also route x16s and x8d interfaces from the XMC site to the VPX backplane.

The XPedite2870 delivers a feature-rich, high-performance platform for interfacing with and processing streaming data from a wide variety of sensors. The X-ES FPGA Development Kit (FDK) provides a pre-validated environment for rapid application development, including an optimized IP library, design resources, software components, and complete example designs for the XPedite2870. The development environment also includes the Arm Trusted Firmware (ATF) and the U-Boot bootloader. Linux Yocto support is available separately.

X-ES
Extreme Engineering Solutions

"Fast, Flexible, Customer-Focused Embedded Solutions"

Extreme Engineering Solutions
9901 Silicon Prairie Parkway • Verona, WI 53593
Phone: 608.833.1155 • Fax: 608.827.6171
sales@xes-inc.com • https://www.xes-inc.com

Adaptive SoC

- AMD Versal® Gen 2 AI Edge 2VE3858 or Prime 2VM3858 adaptive SoC
- Eight Arm® Cortex®-A78AE application processor cores, each with 64 KB instruction L1 cache with parity, 64 KB data L1 cache with ECC, and 512 KB L2 cache; 1 MB L3 cache per two-core cluster; and 4 MB shared system-level cache
- 10 Arm Cortex-R52 real-time processor cores, each with 32 KB L1 cache with ECC and 128 KB tightly coupled memory (TCM) with ECC
- Four-core Arm Mali™-G78AE GPU
- One processing-system high-speed connectivity block supporting configurable combinations of PCIe Gen5, 10GbE, and high-speed debug port (HSDP) interfaces
- Three integrated 100GbE multirate Ethernet MACs (MRMACs)
- Four integrated programmable-logic x4 PCIe Gen5 blocks
- AI Edge 2VE3858 configuration includes 144 AI Engine-ML v2 tiles

Memory

- 32 GB of LPDDR5x SDRAM in four channels
- Up to 256 GB of UFS NAND flash
- 4 Gbit of OSPI FPGA configuration flash

XMC Site

- One x4 PCI Express Gen5-capable interface and rear I/O support

VPX (VITA 46) P0 I/O

- Two IPMB connections to an IPMI controller

VPX (VITA 46) P1 I/O

- Two x4 HSS 25 Gbps-capable interfaces on P1.A and P1.B to support Ethernet, PCIe, etc. (can be combined to function as one x8 PCI Express port)
- Two x1 HSS 25 Gbps-capable interfaces on W15-16 to support 25GBASE-R Ethernet
- One UART/RS-232 maintenance port
- XMC P16 I/O, mapping P1w9-X12d per VITA 46.9

VPX (VITA 46) P2 I/O

- Two 10/100/1000BASE-T Ethernet ports
- Build option for six LVDS GPIO (X5IO)
- One x1 HSS 8 Gbps-capable interface to support PCIe and SATA
- One RS-232/422/485 serial port
- Build option for eight LVDS (X5IO) and 16 single-ended GPIO (HDIO) from the FPGA, or XMC P16 I/O mapping P2w9-X16s+X8d
- Three single-ended GPIO (MIO)

Development Support

- FPGA Development Kit (FDK)
- Arm Trusted Firmware (ATF)
- U-Boot bootloader
- Linux Yocto support

Physical Characteristics

- 3U VPX-REDI conduction- or air-cooled form factor
- Pinout compatible with SOSA I/O Intensive profile (SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16)
- SOSA-aligned to AMPS profile MODA3-16.2.15-1-F2C-(P4F)(P4F)(2E7-E3) (N-D1-U1-N-M3/M4/M5-N)
- Dimensions: 100 mm x 160 mm
- 0.8 in. pitch without solder-side cover
- 0.85 in. and 1.0 in. pitch with solder-side cover and Two-Level Maintenance (2LM) support

Environmental Requirements

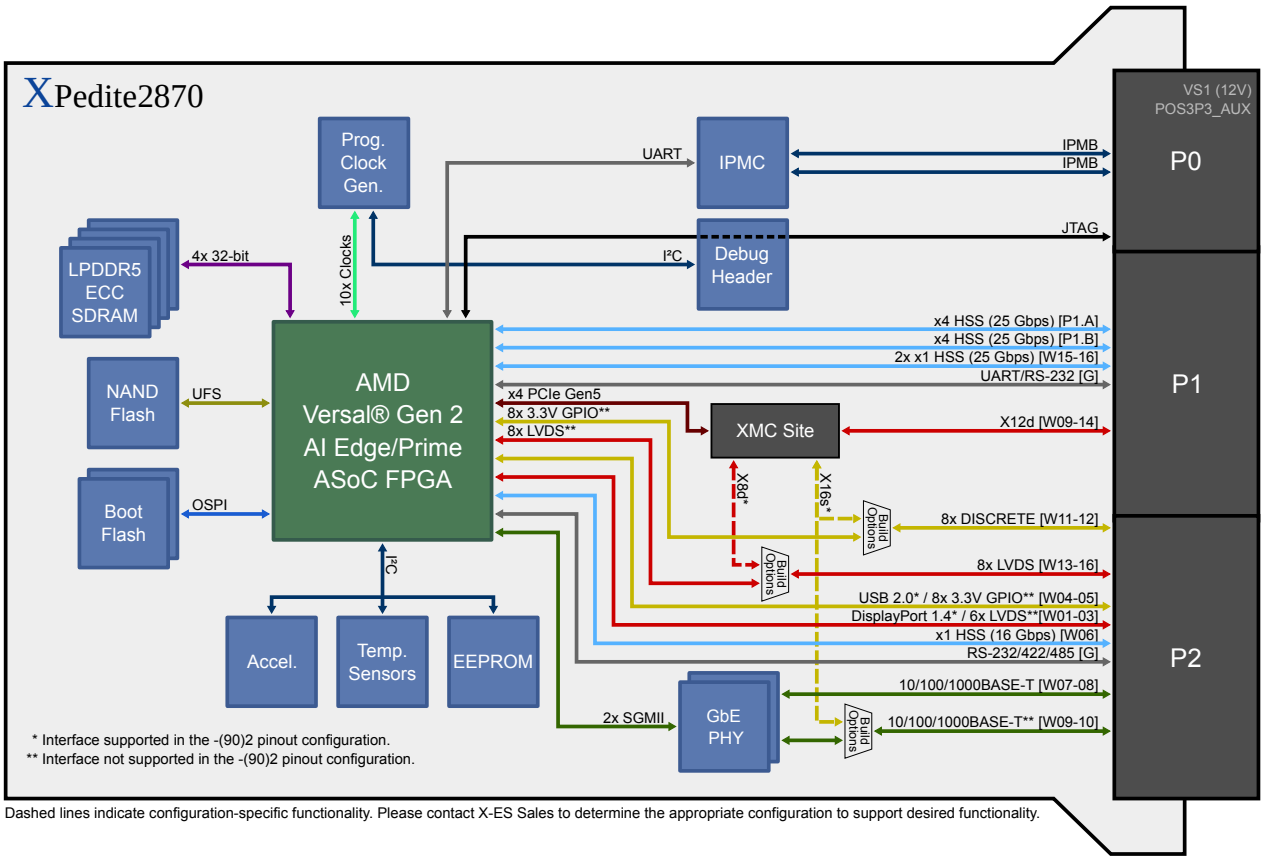
Contact factory for appropriate board configuration based on environmental requirements.

- Supported ruggedization levels (see chart below): 5
- Conformal coating available as an ordering option

Power Requirements

- Power will vary based on configuration and usage. Please consult factory.

Ruggedization Level	**Level 5**
Cooling Method	Conduction-Cooled
Operating Temperature	-40 to +85°C (board rail surface)
Storage Temperature	-55 to +105°C (maximum)
Vibration	0.1 g²/Hz (maximum), 5 to 2000 Hz
Shock	40 g, 11 ms sawtooth
Humidity	Up to 95% non-condensing



Dashed lines indicate configuration-specific functionality. Please contact X-ES Sales to determine the appropriate configuration to support desired functionality.